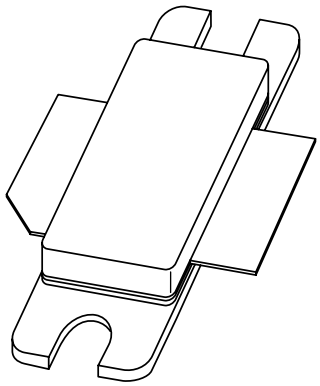
DATA SHEET



BLF1820-90
UHF power LDMOS transistor

Product specification
Supersedes data of 2001 Mar 07

2003 Feb 10

Philips
Semiconductors

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UHF power LDMOS transistor BLF1820-90

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 500 mA:
  - Output power = 90 W (PEP)
  - Gain = 12 dB
  - Efficiency = 32%
  - dim = –26 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (1800 to 2000 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the 1800 to 2000 MHz frequency range.

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

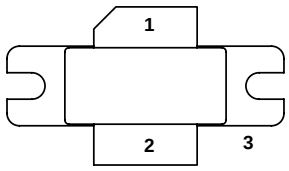


Fig.1 Simplified outline SOT502A.

DESCRIPTION

90 W LDMOS power transistor for base station applications at frequencies from 1800 to 2000 MHz.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	90 (PEP)	>11	>30	≤–25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	12	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C; note 1	0.81	K/W

Note

1. Determined under specified RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 2.1 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 210 mA	4.4	–	5.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	15	μA
I_{DSX}	on-state drain current	V_{GS} =V_{GSth} + 9 V; V_{DS} = 10 V	27	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	38	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	–	6.2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 7.5 A	–	0.1	–	Ω
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz; note 1	–	5.1	–	pF

Note

1. The value of capacitance is that of the die only.

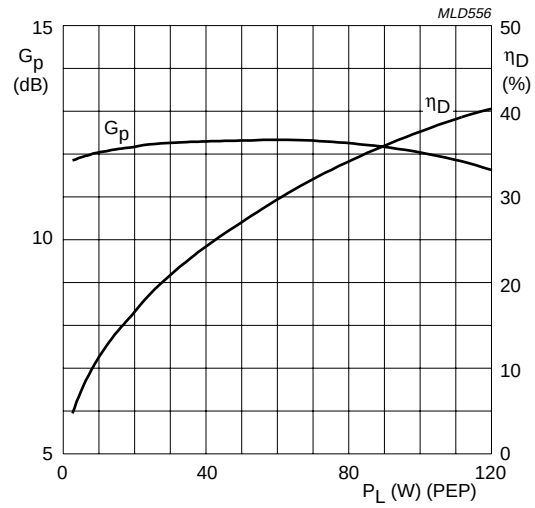
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 0.81 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
Two-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	750	90 (PEP)	>11	>30	≤–25

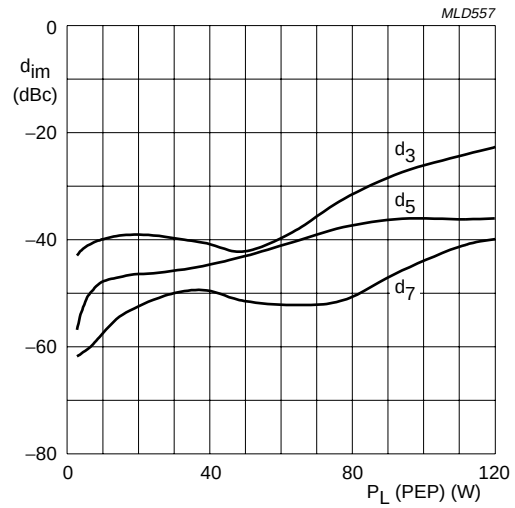
Ruggedness in class-AB operation

The BLF1820-90 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; I_{DQ} = 750 mA; P_L = 90 W; f = 2000 MHz (single tone).



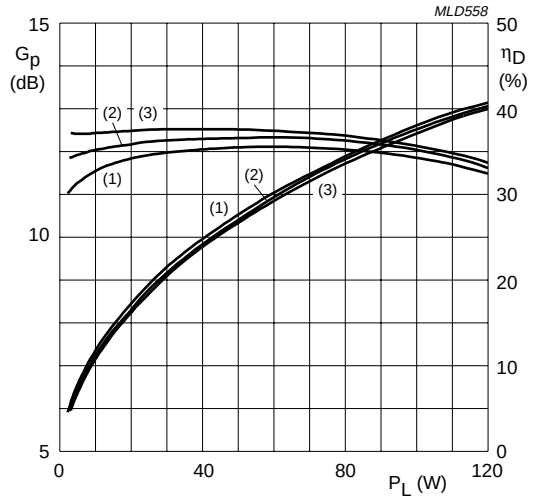
V_{DS} = 26 V; I_{DQ} = 750 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 750 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

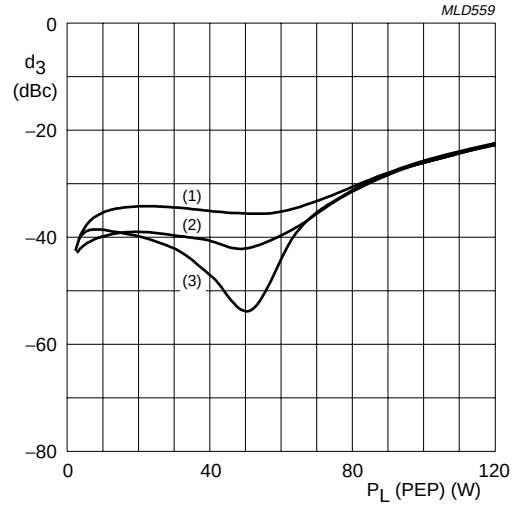
Fig.3 Intermodulation distortion products as functions of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 750 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

(1) I_{DQ} = 600 mA. (2) I_{DQ} = 750 mA. (3) I_{DQ} = 900 mA.

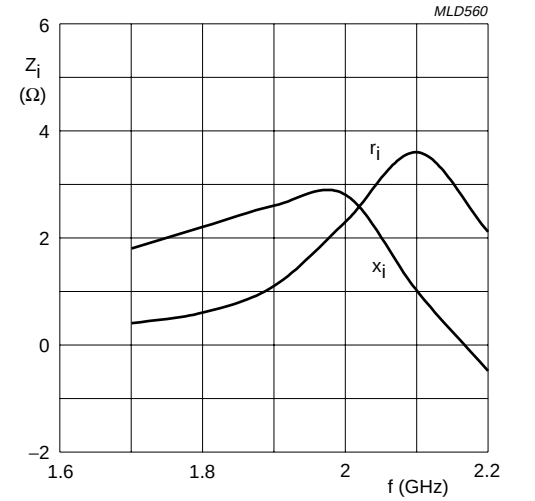
Fig.4 Power gain and drain efficiency as functions of average load power; typical values.



V_{DS} = 26 V; I_{DQ} = 750 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

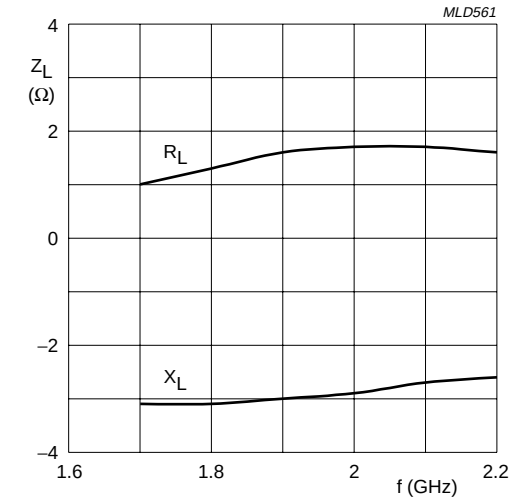
(1) I_{DQ} = 600 mA. (2) I_{DQ} = 750 mA. (3) I_{DQ} = 900 mA.

Fig.5 Intermodulation distortion products as functions of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 750 mA; P_L = 90 W; $T_h \leq 25$ °C.

Fig.6 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 750 mA; P_L = 90 W; $T_h \leq 25$ °C.

Fig.7 Load impedance as a function of frequency (series components); typical values.

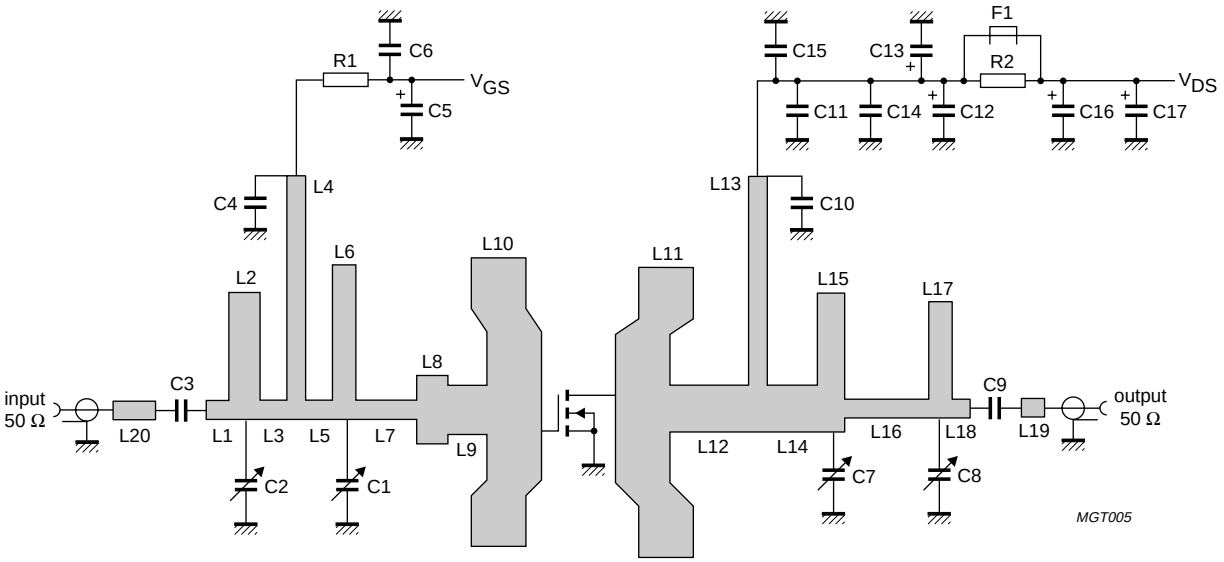


Fig.8 2 GHz class-AB test circuit.

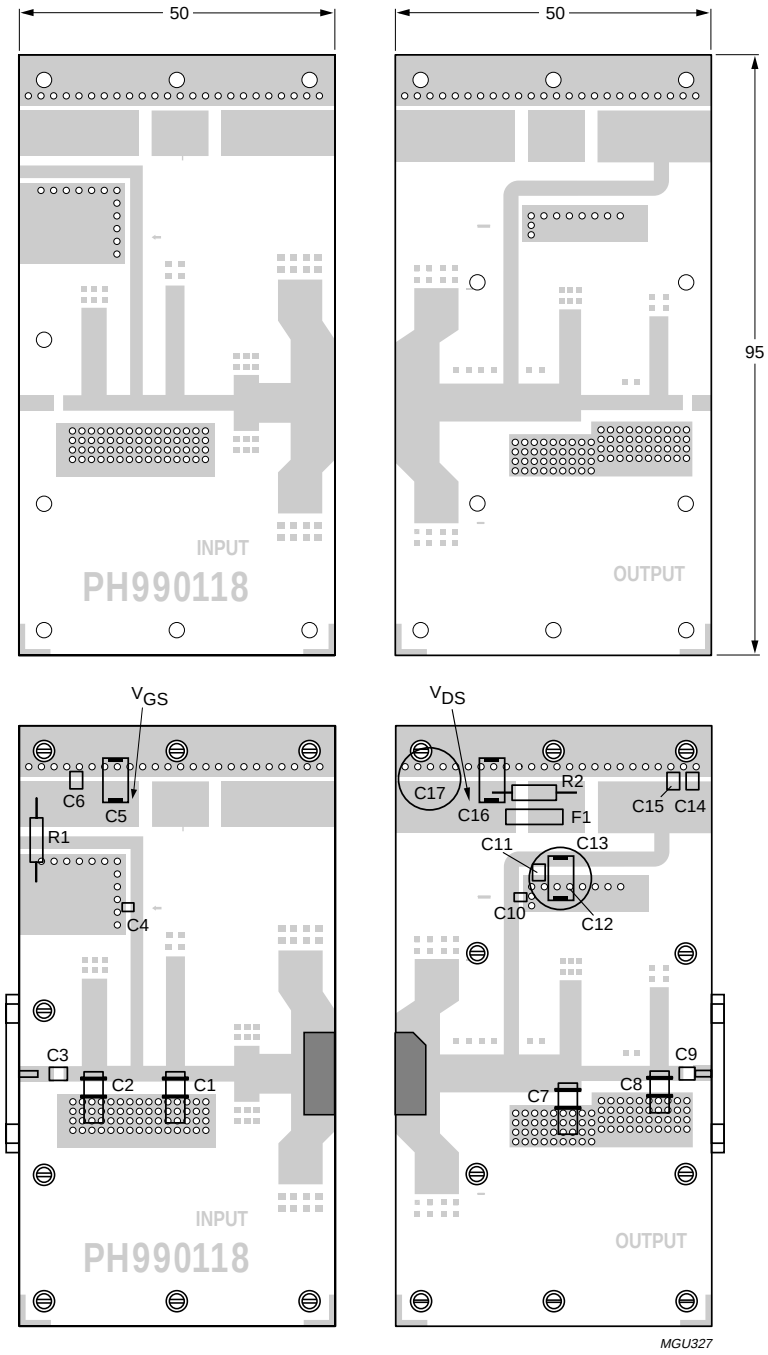
List of components

See Figs 8 and 9.

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7, C8	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C3, C9	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C10	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12, C16	electrolytic capacitor	4.5 μF; 50 V		
C6, C11, C15	multilayer ceramic chip capacitor; note 1	1 nF		
C13, C17	electrolytic capacitor	100 μF; 63 V		2222 037 58101
C14	multilayer ceramic chip capacitor	100 nF		2222 581 16641
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 × 2.4 mm	
L2		10.8 Ω	4 × 16.3 mm	
L3		50 Ω	3.7 × 2.4 mm	
L4		6 Ω	2 × 30.8 mm	
L5		50 Ω	3.6 × 2.4 mm	
L6		9 Ω	3 × 19.9 mm	
L7		50 Ω	7.8 × 2.4 mm	
L8		18.5 Ω	4 × 8.8 mm	
L9		24.4 Ω	5 × 6.3 mm	
L10		5.1 Ω	7 × 37 mm	
L11		5.1 Ω	7 × 40.9 mm	
L12		25.4 Ω	10.1 × 6 mm	
L13		5.7 Ω	2.4 × 32.8 mm	
L14		25.4 Ω	6.4 × 6 mm	
L15		10 Ω	3.5 × 20.7 mm	
L16		50 Ω	10.8 × 2.4 mm	
L17		11.8 Ω	3 × 7.9 mm	
L18		50 Ω	2.3 × 2.4 mm	
L19		50 Ω	3 × 2.4 mm	
L20		50 Ω	5.5 × 2.4 mm	
R1, R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2); thickness 0.79 mm.



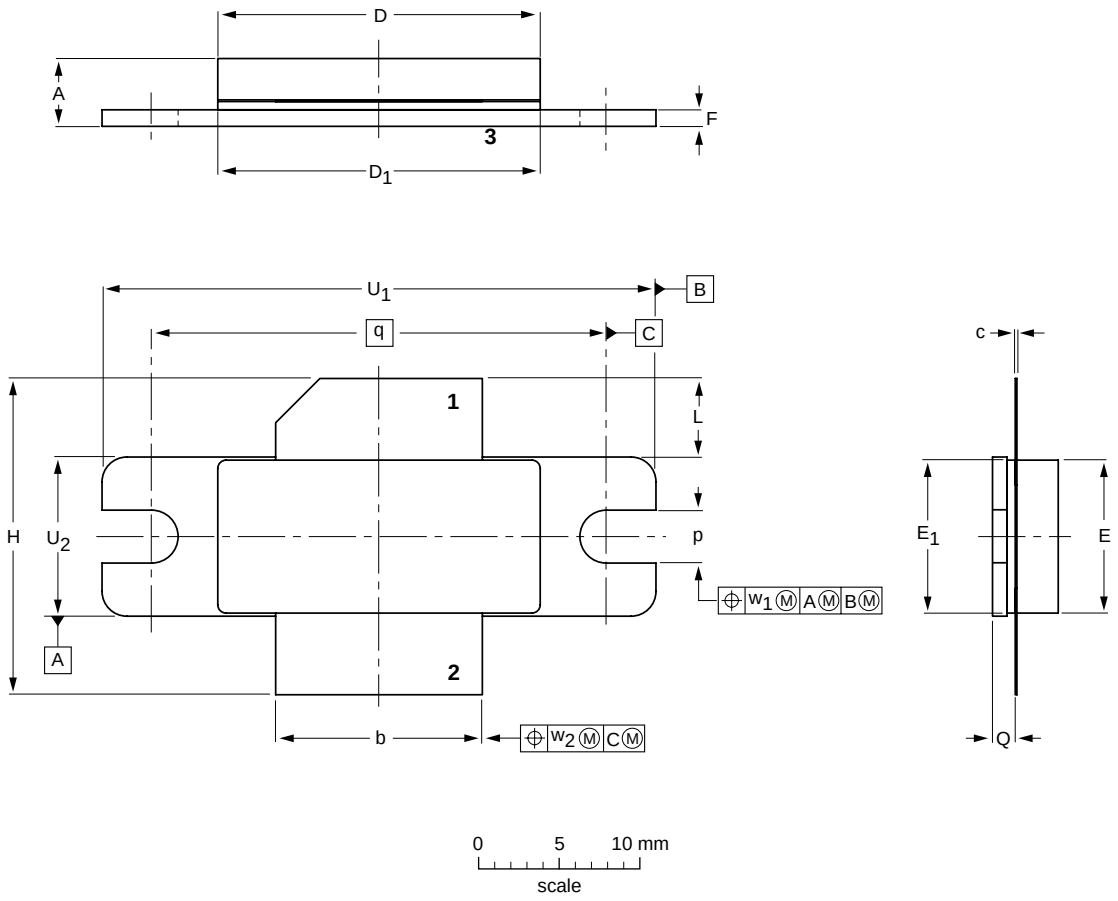
Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2 GHz class-AB test circuit.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

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Printed in The Netherlands 613524/02/pp12 Date of release: 2003 Feb 10 Document order number: 9397 750 10916

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